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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/574,775	04/06/2006	Sougo Ohta	071971-0460	2530

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EXAMINER	
HSIEH, HSIN YI	
ART UNIT	**PAPER NUMBER**
2811	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/574,775	OHTA ET AL.	
	Examiner	Art Unit	
	Hsin-Yi (Steven) Hsieh	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 February 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 February 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *20080201*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on 02/01/2008 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claim 14 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 14 recites the limitation "a row-select unit formed on the substrate, and a column-select unit formed on the substrate" in the second and the third lines of the claim. There is no support in the specification for these structure relationships, while the row-select unit and the column-select unit can be formed in another chip and not on the substrate having the transfer transistors.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. **Claims 8-13** are rejected under 35 U.S.C. 102(b) as being anticipated by Guidash (US 6,657,665 B1).

5. Regarding **claim 8**, Guidash teaches a solid-state imaging apparatus (image sensor; Abstract) comprising: a substrate (semiconductor substrate; Abstract) ; a first pixel (upper pixel 10; Fig. 4, col. 3 line 48) formed on the substrate (Abstract) including a first photodiode (photodiode photodetectors 12 in the first pixel; Fig. 4, col. 3 lines 57-58), a first transfer transistor (the transistor formed with the transfer gate 23 in the first pixel; Fig. 4, col. 3 line 58) and a first floating diffusion (25 in the first pixel; Fig. 4, col. 3 line 58); a second pixel (lower pixel 10; Fig. 4, col. 3 line 48) formed on the substrate (Abstract) adjacent to the first pixel (upper 10) including a second photodiode (photodiode photodetectors 12 in the second pixel; Fig. 4, col. 3 lines 57-58), a second transfer transistor (the transistor formed with the transfer gate 23 in the second pixel; Fig. 4, col. 3 line 58) and a second floating diffusion (25 in the second pixel; Fig. 4, col. 3 line 58); a reset transistor (14; Fig. 4, col. 3 line 59) formed on the substrate (Abstract); and an amplifier transistor (source follower input signal transistor 21; Fig. 4, col. 3 lines 59-60) formed on the substrate (abstract), wherein a gate electrode (SIG; Fig. 4) of the amplifier transistor (21) is connected to the first floating diffusion (25 in upper 10; see Fig. 4 and

col. 4, lines 1-4) and the second floating diffusion (25 in lower 10; see Fig. 4 and col. 4, lines 1-4), a source (the lower source/drain region) of the reset transistor (15) is connected to the first floating diffusion (25 in the upper 10; through the 25 in the lower 10 and conductive interconnect layer 44; see Fig. 4 and col. 4, lines 1-4) and the source (the lower source/drain region) of the reset transistor (15) is connected to the second floating diffusion (25 in the lower 10; see Fig. 4), and a distance and direction (the distance in the horizontal direction) from the first photodiode (PDa in Fig. 4) to the first floating diffusion (FDa in Fig 4; the distance between the right end of PDa and the left end of FDa) are substantially equal to a distance and direction (the distance in the horizontal direction) from the second photodiode (PDb in Fig. 4) to the second floating diffusion (FDb in Fig 4; the distance between the right end of PDb and the left end of FDb).

6. Regarding **claim 9**, Guidash also teaches the solid-state imaging apparatus of claim 8, further comprising: a power supply interconnect (voltage supply 8; Fig. 4, col. 3 line 60); and an output interconnect (row select gate transistor 30 with a row select gate (RSG) 31; Fig. 4, col. 3 line 62), wherein the power supply interconnect (8) is connected to a drain (the upper source/drain region) of the reset transistor (15; see Fig. 4) and a source (the lower source/drain) of the amplifier transistor (21; see Fig. 4), and the output interconnect (30) is connected to a drain (the upper source/drain region) of the amplifier transistor (21; 30 and 21 share one source/drain region, see Fig. 4).

7. Regarding **claim 10**, Guidash also teaches the solid-state imaging apparatus of claim 8, wherein the amplifier transistor (21) is formed in the first pixel (upper 10; the majority part of 21 is in the upper pixel 10), the reset transistor (14) is formed in the second pixel (lower 10, see Fig. 4), and a distance and direction (a distance in the horizontal direction) from the first photodiode

(PDa in Fig. 4) to the amplifier transistor (21; the distance between the right end of PDa and the left end of the gate of 21) are substantially equal to a distance and direction (a distance in the horizontal direction) from the second photodiode (PDb in Fig. 4) to the reset transistor (14; the distance between the right end of PDb and the left end of the gate of 14).

8. Regarding **claim 11**, Guidash also teaches the solid-state imaging apparatus of claim 8, wherein a shape and size of the first pixel (upper 10) are substantially equal to a shape and size as that of the second pixel (lower 10; see Fig. 4).

9. Regarding **claim 12**, Guidash also teaches the solid-state imaging apparatus of claim 8, wherein the solid-state imaging apparatus comprises a plurality of units (the unit of two pixel 10s shown in Fig. 4), and each of the units includes only the first pixel (the upper 10), the second pixel (the lower 10), the reset transistor (14) and the amplifier transistor (21).

10. Regarding **claim 13**, Guidash also teaches the solid-state imaging apparatus of claim 8, wherein the amplifier transistor (21) and the reset transistor (14) are formed in the second pixel (the lower pixel 10; part of 21 is in the lower pixel 10) and a drain (the upper source/drain region) of the reset transistor (14) is a source (the lower source/drain region) of the amplifier transistor (21; 21 and 14 share one source/drain region).

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

13. **Claim 14** is rejected under 35 U.S.C. 103(a) as being unpatentable over Guidash as applied to claim 8 above, and further in view of Shinohara et al. (US 2004/0000681 A1) as can be understood since claims 14 have been rejected under 35 U.S.C. 112.

14. Regarding **claim 14**, Guidash does not teach a row-select unit formed on the substrate, and a column-select unit formed on the substrate, wherein gates of the first transfer transistor and the second transfer transistor are connected to the row select unit, and a drain of the amplifier transistor is connected to the column-select unit.

In the same field of endeavor of Active Pixel Sensors, Shinohara et al. teaches a row-select unit (vertical scan circuit 1110, Fig 11; paragraph [0120]) formed on the substrate (can be integrated, i.e. sharing the same substrate of chip, as peripheral circuits; paragraph [0004-0005]), and a column-select unit (horizontal scan circuit 1117, Fig 11; paragraph [0121]) formed on the substrate (can be integrated, i.e. sharing the same substrate of chip, as peripheral circuits; paragraph [0004-0005]), wherein gates of the first transfer transistor and the second transfer transistor (gates of multiple transfer MOS transistors 1103, Fig 11; paragraph [0120]) are connected to the row select unit (vertical scan circuit 1110, Fig 11; paragraph [0120]; connected

through the transfer line 1109), and a drain of the amplifier transistor (drain of amplifying MOS transistor 1104; Fig 11, paragraph [0120]) is connected to the column-select unit (horizontal scan circuit 1117, Fig 11; paragraph [0121]; connected through the output line 1111). Shinohara et al. also teach that the row-select unit and the column-select unit are parts of the circuits to read out an array of pixels (paragraph [0120]).

It would have been obvious to one of ordinary skill in the art at the time of invention was made to combine the inventions of Guidash and Shinohara et al. and use the row-select unit and the column-select unit as taught by Shinohara et al., because they are the necessary parts of the circuits to read out an array of pixels as taught by Shinohara et al.

Response to Arguments

15. Applicant's amendments, filed 02/01/2008, overcome the objections to the drawings, the title, and the rejections to claims 1-7 under 35 U.S.C. 112. The objections to the objections to the drawings, the title, and the rejections to claims 1-7 under 35 U.S.C. 112 have been withdrawn.

16. Applicant's arguments filed 02/01/2008 have been fully considered but they are not persuasive.

17. On page 9 of the Applicant's Response, Applicant argues that Guidash fails to teach a distance and direction from the first photodiode to the first floating diffusion are substantially equal to a distance and direction from the second photodiode to the second floating diffusion.

18. The examiner respectfully disagrees with Applicant's argument. Guidash teaches a distance and direction from the first photodiode to the first floating diffusion are substantially

equal to a distance and direction from the second photodiode to the second floating diffusion, which is clearly stated in the art rejection.

Conclusion

19. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsin-Yi (Steven) Hsieh whose telephone number is 571-270-3043. The examiner can normally be reached on Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne A. Gurley can be reached on 571-272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Lynne A. Gurley/
Supervisory Patent Examiner, Art Unit 2811

/H. H./
Examiner, Art Unit 2811
4/28/2008